FIG.1

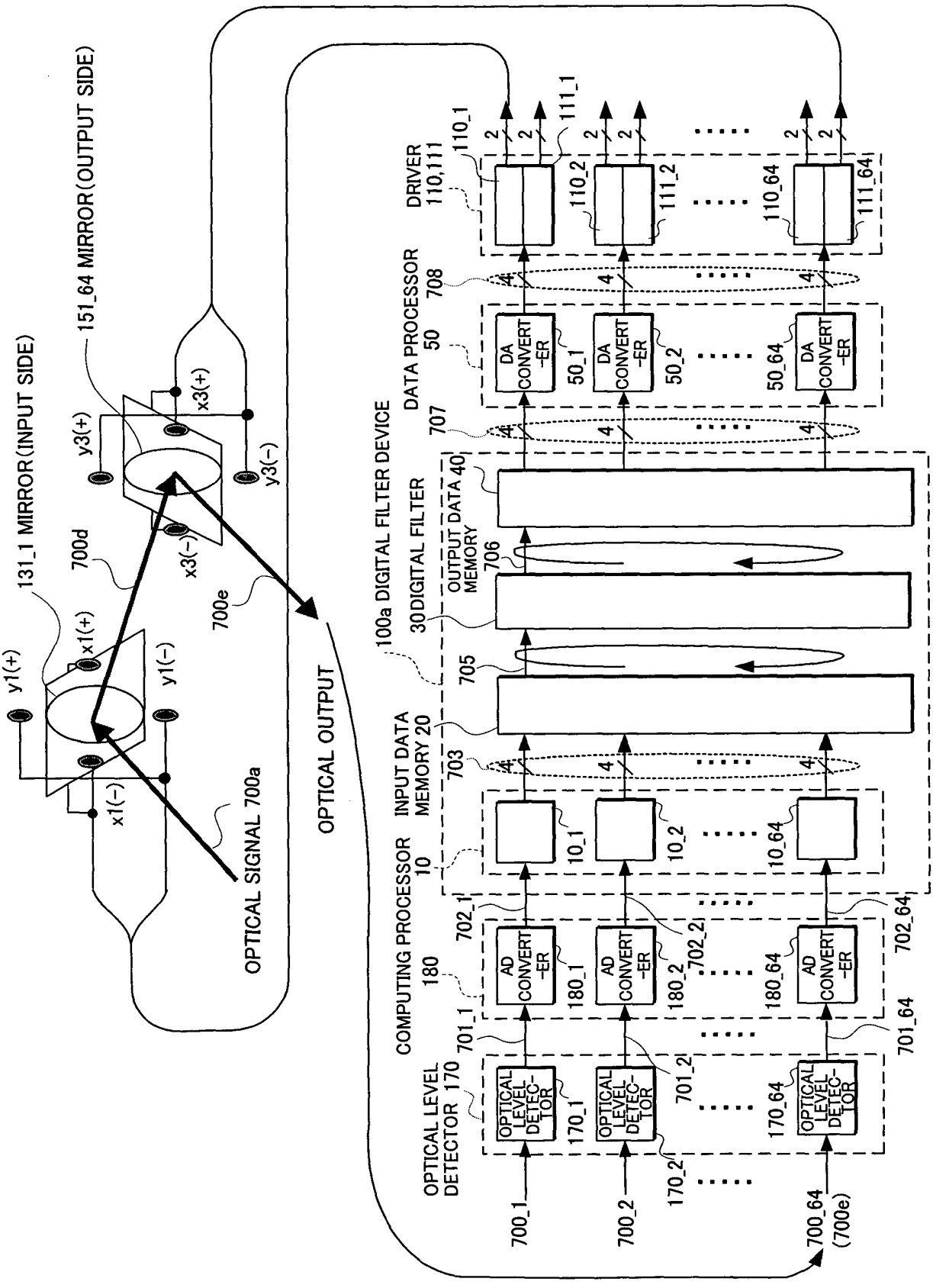
131_1 MIRROR(INPUT SIDE)
151_64 MIRROR(OUTPUT SIDE)
y1(+)
x1(+)
y1(-)
x1(-)
700d
y3(+)
x3(+)
x3(-)
y3(-)
700e
OPTICAL SIGNAL 700a
OPTICAL OUTPUT
100a DIGITAL FILTER DEVICE
COMPUTING PROCESSOR 10
INPUT DATA MEMORY 20
30DIGITAL FILTER
OUTPUT DATA MEMORY 706
DATA PROCESSOR 50
DRIVER 110,111
OPTICAL LEVEL DETECTOR 170
AD CONVERTER
DA CONVERTER
OPTICAL LEVEL DETECTOR
700_1
700_2
700_64 (700e)
705
707
708
703
180
701_1
701_64
702_1
702_64
170_1
170_2
170_64
180_1
180_2
180_64
10_1
10_2
10_64
50_1
50_2
50_64
110_1
110_2
110_64
111_1
111_2
111_64

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FIG.2

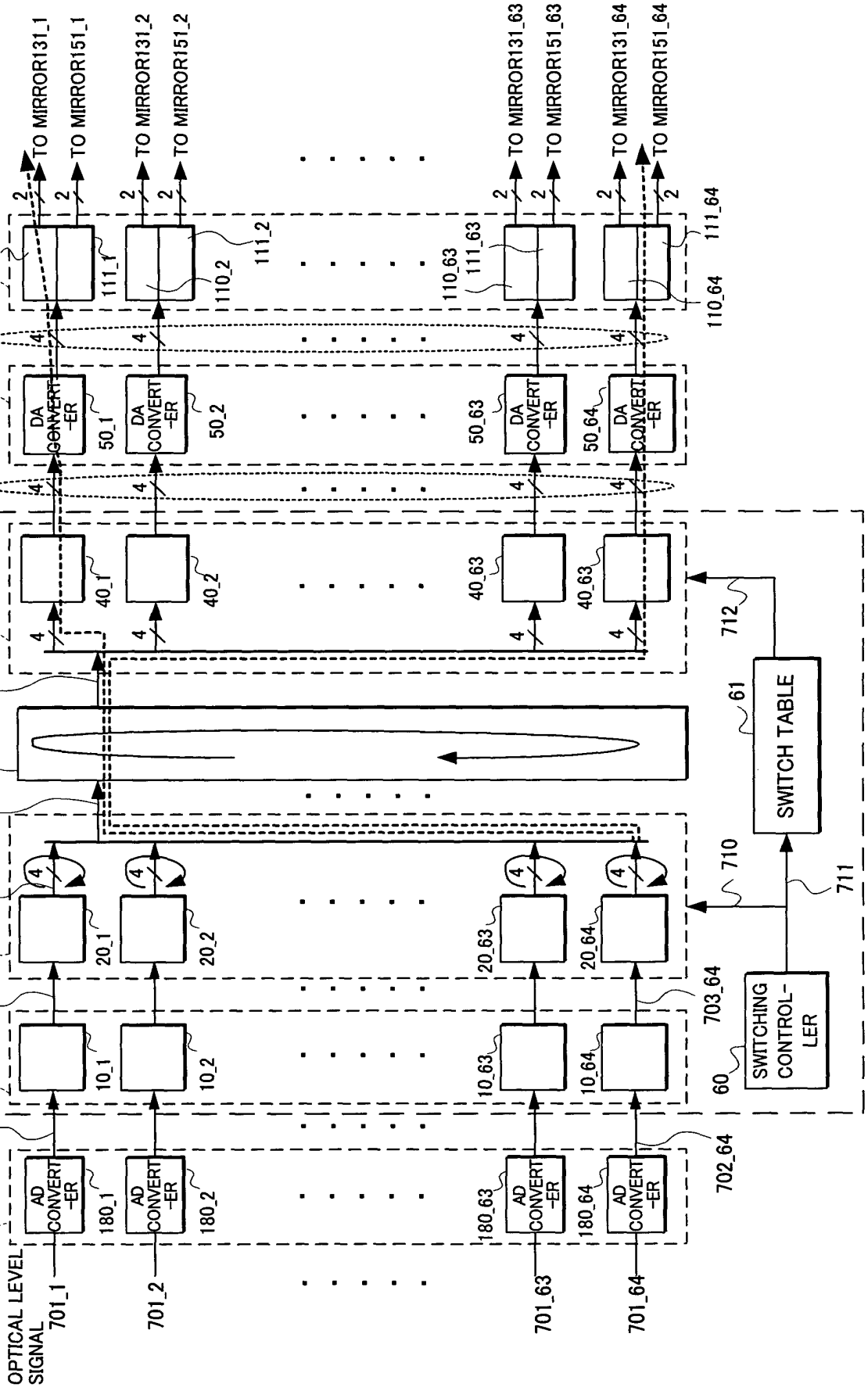
100b DIGITAL FILTER DEVICE
OPTICAL LEVEL SIGNAL
701_1
701_2
701_63
701_64
180
AD CONVERTER
180_1
180_2
180_63
180_64
COMPUTING PROCESSOR
10
702_1
702_64
10_1
10_2
10_63
10_64
703_1
703_64
INPUT DATA MEMORY
20
704_1
20_1
20_2
20_63
20_64
DIGITAL FILTER
30
705
706
OUTPUT DATA MEMORY
40
40_1
40_2
40_63
40_64
707
708
50
DA CONVERTER
50_1
50_2
50_63
50_64
110,111 DRIVER
110_1
110_2
110_63
110_64
111_1
111_2
111_63
111_64
TO MIRROR131_1
TO MIRROR151_1
TO MIRROR131_2
TO MIRROR151_2
TO MIRROR131_63
TO MIRROR151_63
TO MIRROR131_64
TO MIRROR151_64
SWITCHING CONTROLLER
60
SWITCH TABLE
61
710
711
712

FIG.3

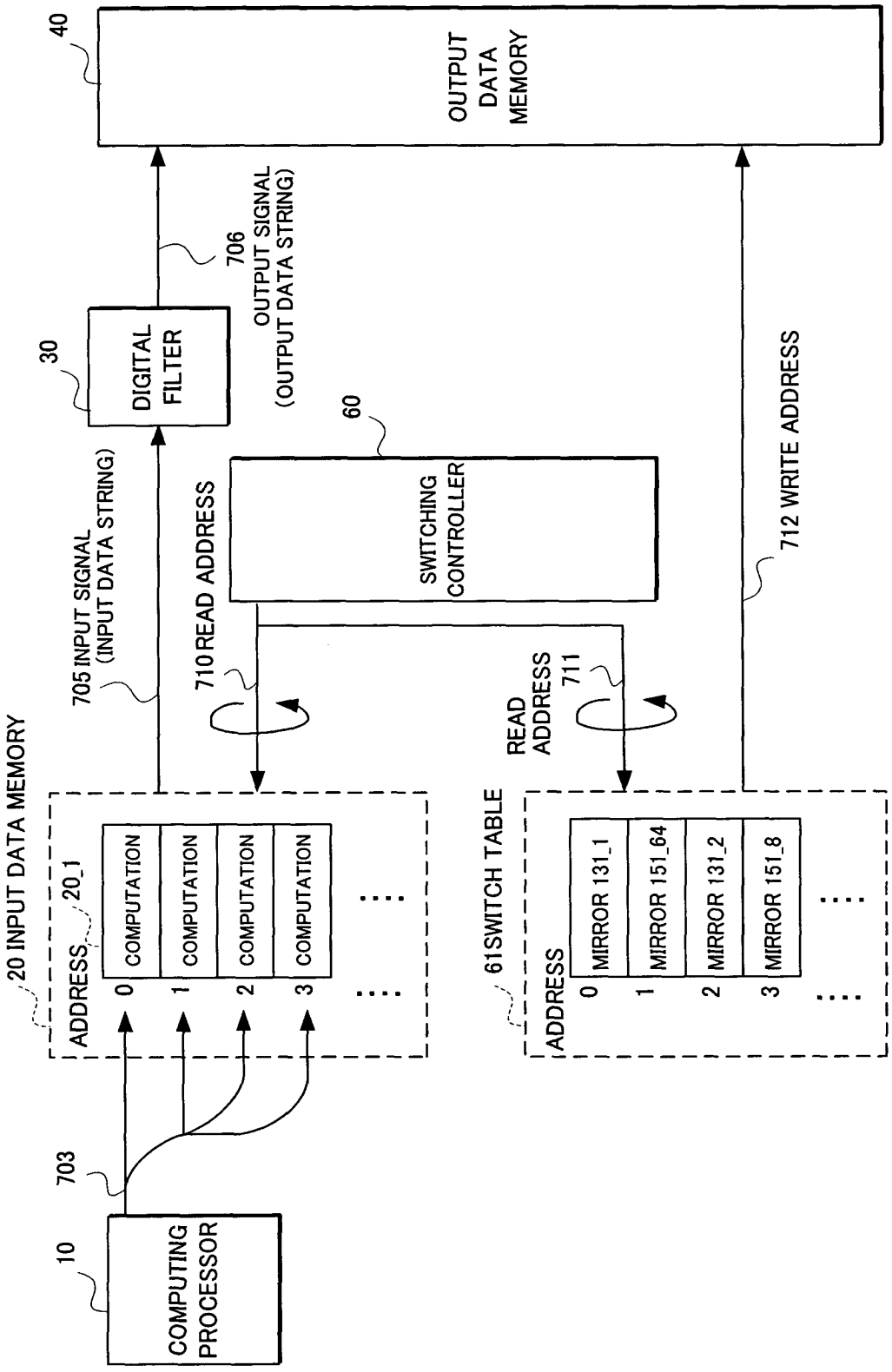
40
OUTPUT DATA MEMORY
706 OUTPUT SIGNAL (OUTPUT DATA STRING)
30
DIGITAL FILTER
60
SWITCHING CONTROLLER
705 INPUT SIGNAL (INPUT DATA STRING)
710 READ ADDRESS
READ ADDRESS 711
712 WRITE ADDRESS
20 INPUT DATA MEMORY
20_1
ADDRESS
0 COMPUTATION
1 COMPUTATION
2 COMPUTATION
3 COMPUTATION
61 SWITCH TABLE
ADDRESS
0 MIRROR 131_1
1 MIRROR 151_64
2 MIRROR 131_2
3 MIRROR 151_8
703
10
COMPUTING PROCESSOR

FIG.4A

PROCESSING CYCLE
ADDRESS 710
(INPUT DATA MEMORY
READ ADDRESS)

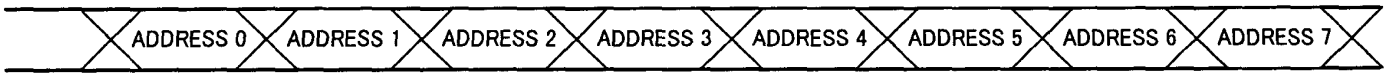

FIG.4B

SWITCH TABLE READ
ADDRESS 711

FIG.4C

SWITCH TABLE DATA 712
(OUTPUT DATA MEMORY
WRITE ADDRESS)

FIG.4D

FILTER MEMORY
WRITE ADDRESS 713
READ ADDRESS 714

FIG.4E

WRITE DATA 715 OF
FILTER MEMORY

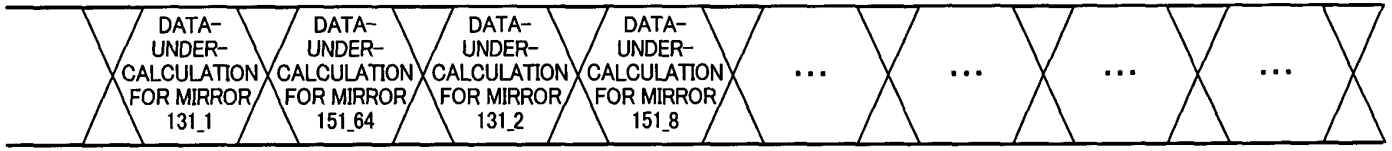

FIG.4F

READ DATA 716 OF
FILTER MEMORY

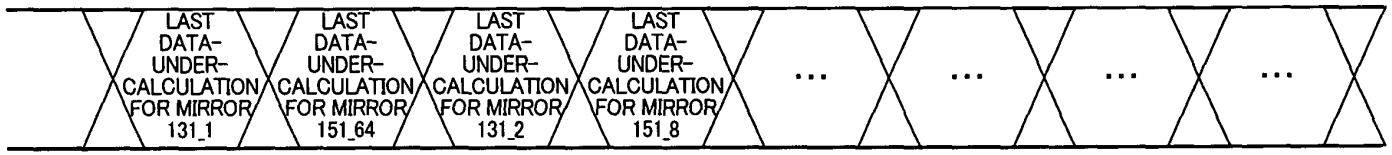

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FIG.5

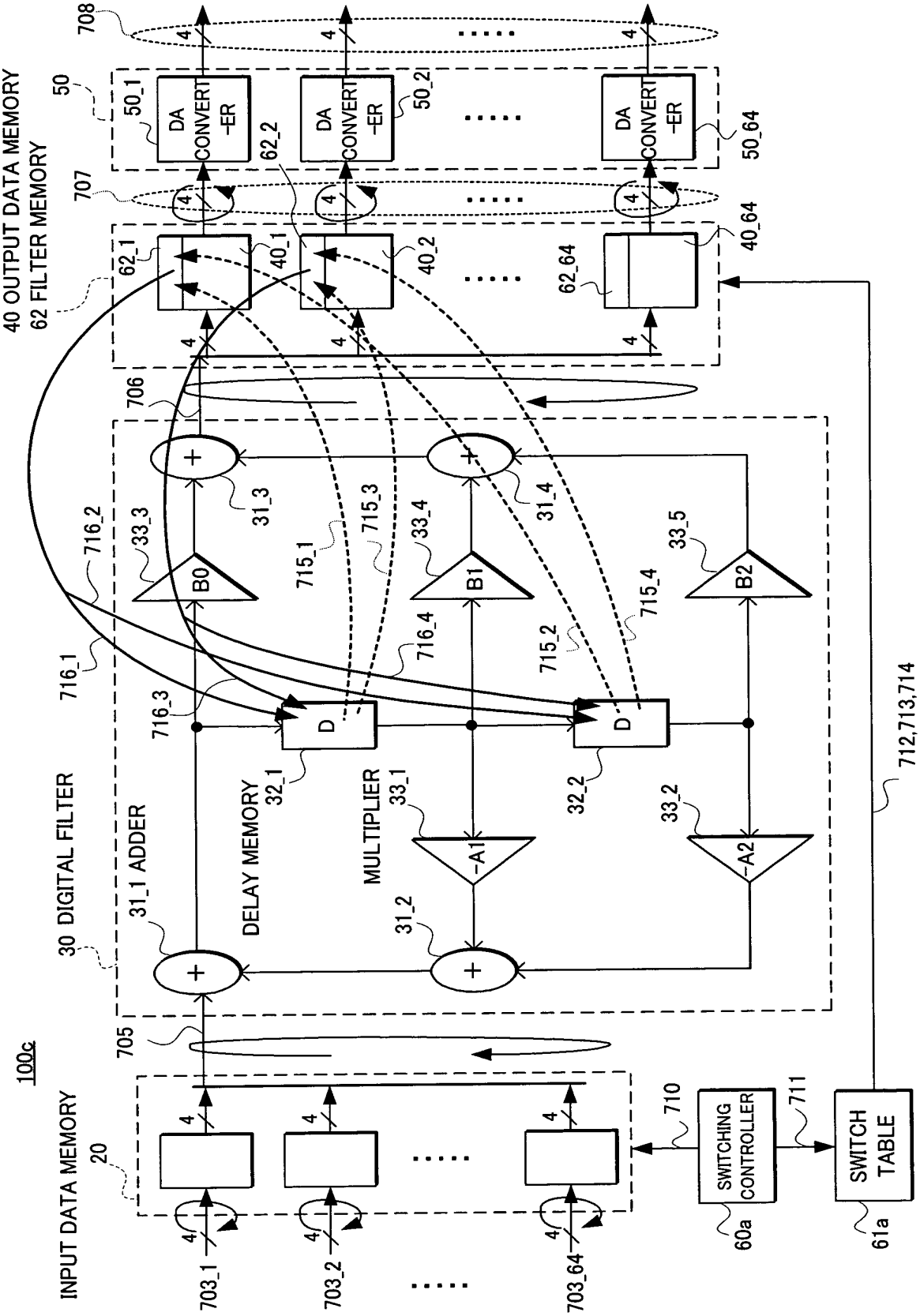

100c
INPUT DATA MEMORY
20
703_1
703_2
703_64
705
30 DIGITAL FILTER
31_1 ADDER
DELAY MEMORY
32_1
32_2
MULTIPLIER
33_1
33_2
33_3
33_4
33_5
B0
B1
B2
-A1
-A2
31_1
31_2
31_3
31_4
706
707
708
40 OUTPUT DATA MEMORY
62 FILTER MEMORY
62_1
62_2
62_64
40_1
40_2
40_64
50
50_1
50_2
50_64
DA CONVERTER
716_1
716_2
716_3
716_4
715_1
715_2
715_3
715_4
710
SWITCHING CONTROLLER
60a
711
SWITCH TABLE
61a
712,713,714

FIG.6

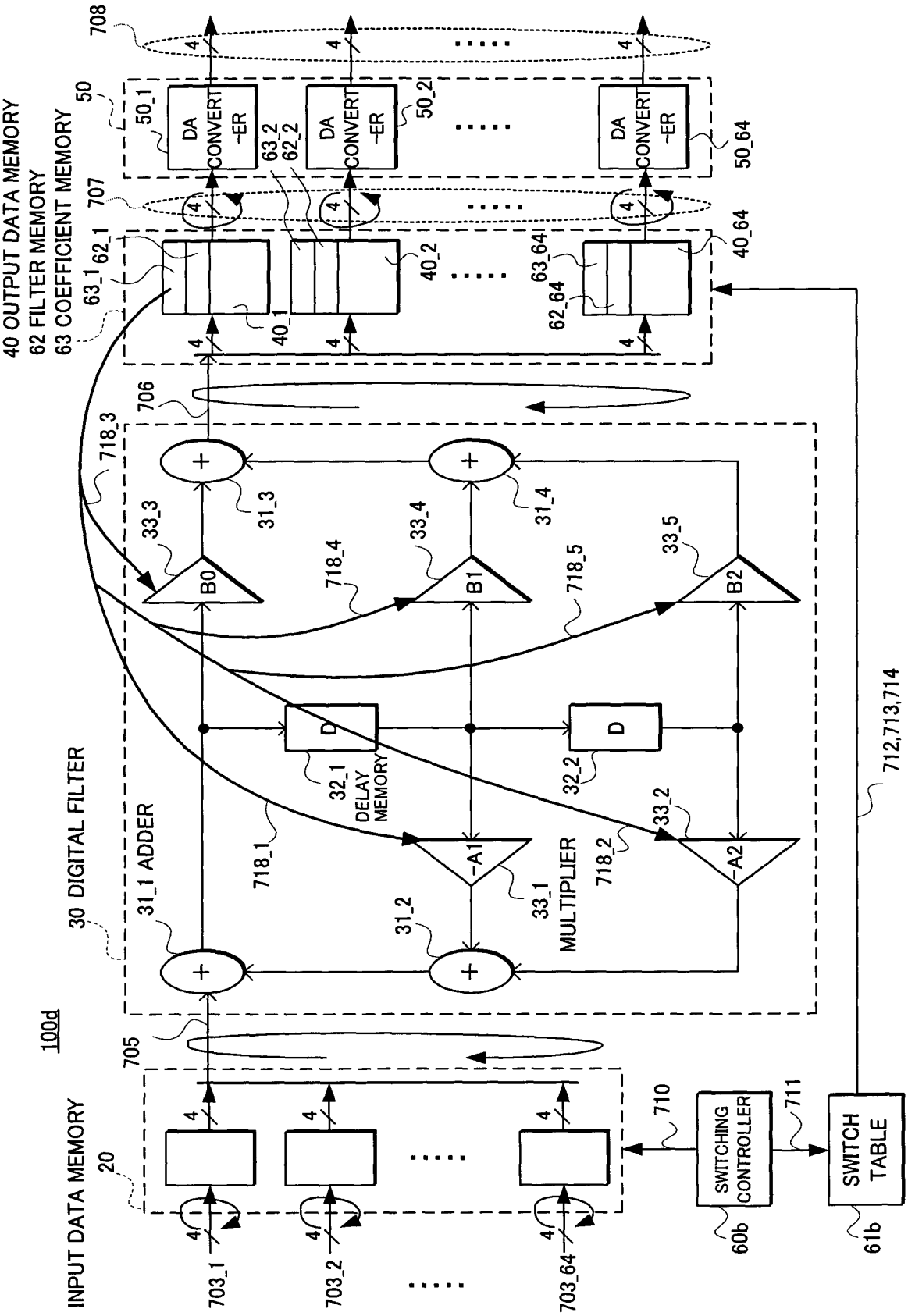
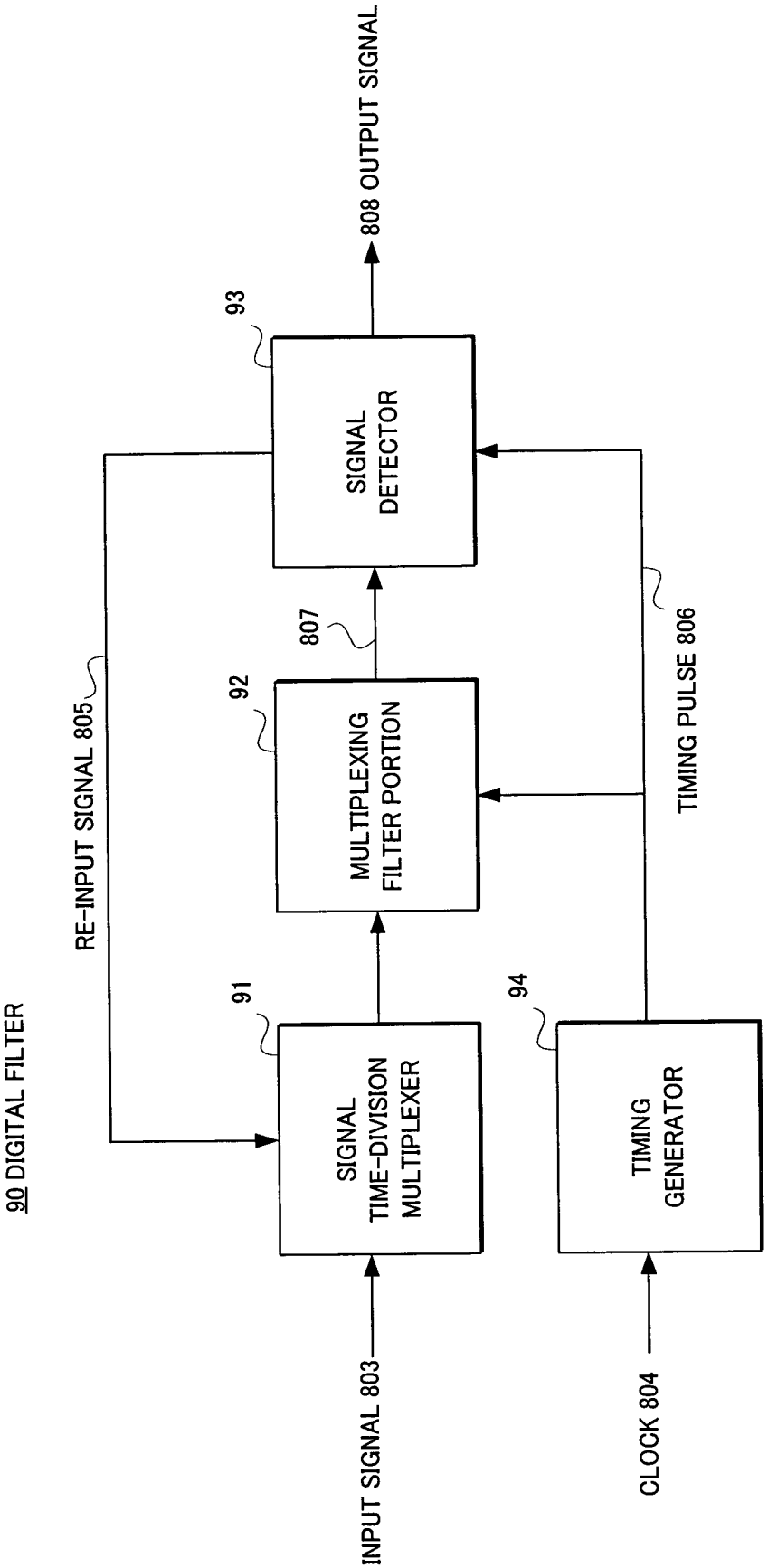

100d
INPUT DATA MEMORY
20
703_1
703_2
703_64
705
30 DIGITAL FILTER
31_1 ADDER
31_2
31_3
31_4
718_1
718_2
718_3
718_4
718_5
32_1
DELAY MEMORY
32_2
33_1
MULTIPLIER
33_2
33_3
33_4
33_5
B0
B1
B2
-A1
-A2
D
706
40 OUTPUT DATA MEMORY
62 FILTER MEMORY
63 COEFFICIENT MEMORY
707
708
50
50_1
50_2
50_64
DA CONVERTER
63_1
62_1
63_2
62_2
63_64
62_64
40_1
40_2
40_64
710
711
712,713,714
SWITCHING CONTROLLER
60b
SWITCH TABLE
61b

FIG.7
PRIOR ART



FG161

FIG.8
PRIOR ART

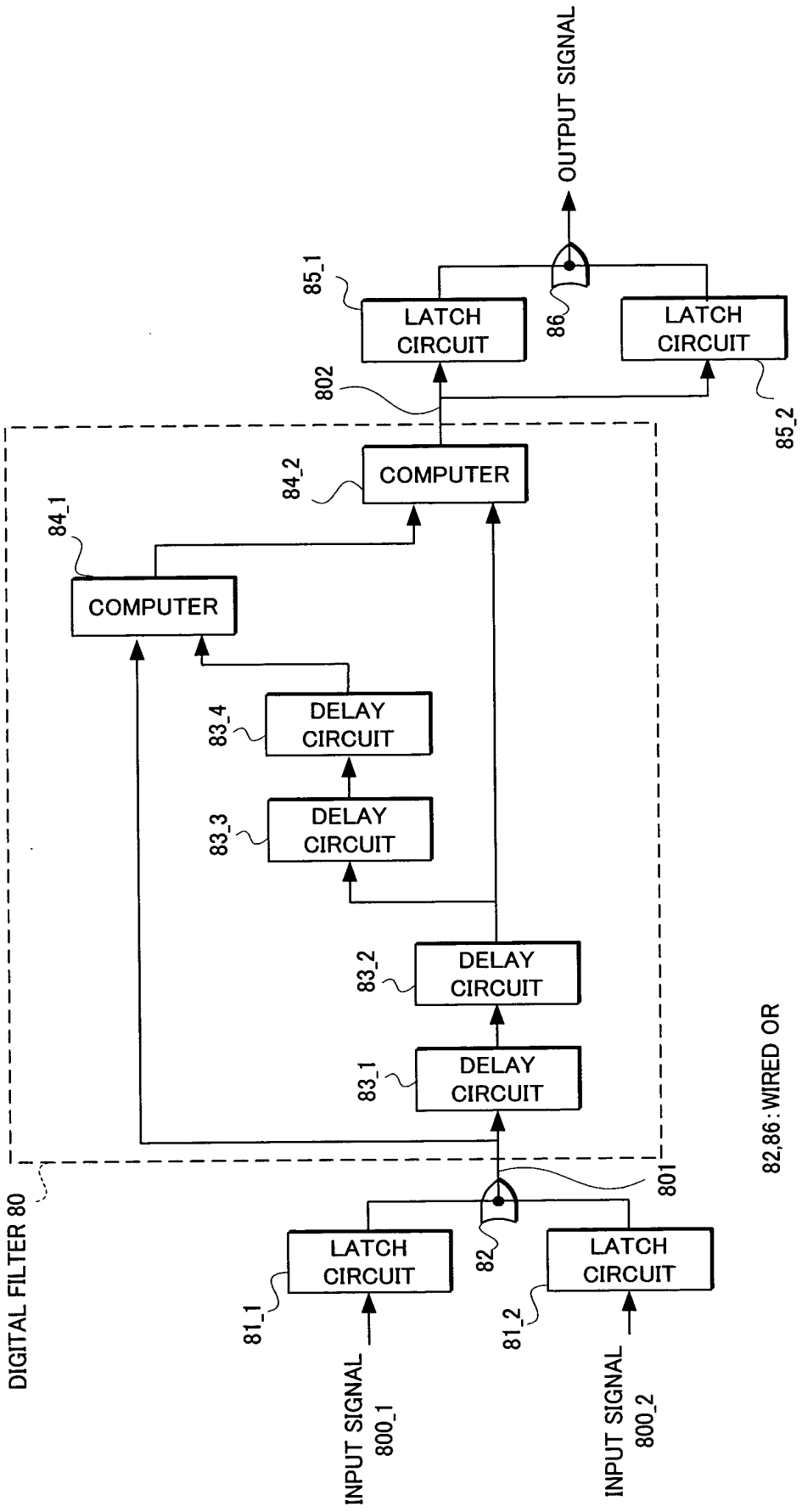


FIG.9

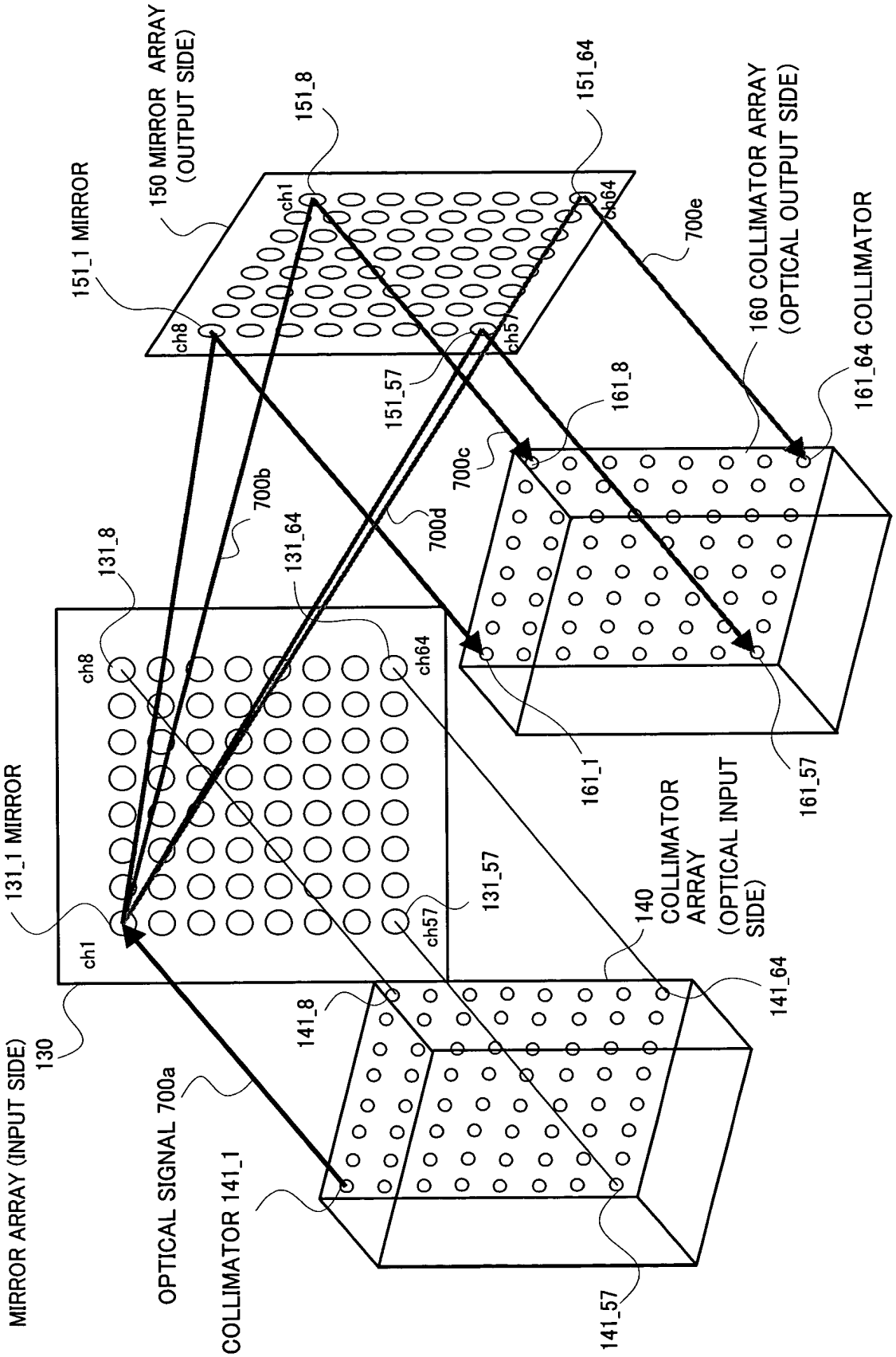
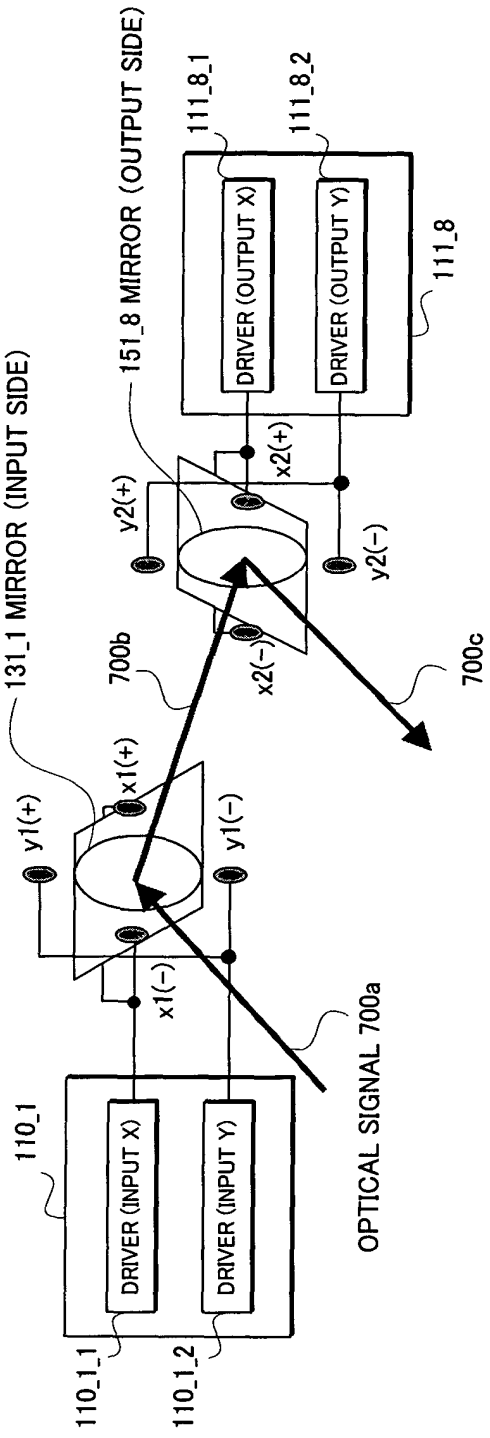

MIRROR ARRAY (INPUT SIDE)
130
131_1 MIRROR
ch1
ch8
131_8
131_64
ch64
131_57
ch57
OPTICAL SIGNAL 700a
COLLIMATOR 141_1
141_8
141_64
141_57
140
COLLIMATOR
ARRAY
(OPTICAL INPUT
SIDE)
700b
700c
700d
700e
150 MIRROR ARRAY
(OUTPUT SIDE)
151_1 MIRROR
151_8
151_64
151_57
161_1
161_8
161_57
160 COLLIMATOR ARRAY
(OPTICAL OUTPUT SIDE)
161_64 COLLIMATOR

FIG.10


131_1 MIRROR (INPUT SIDE)
151_8 MIRROR (OUTPUT SIDE)
110_1
DRIVER (INPUT X)
DRIVER (INPUT Y)
110_1_1
110_1_2
111_8
111_8_1
111_8_2
DRIVER (OUTPUT X)
DRIVER (OUTPUT Y)
x1(+)
x1(-)
y1(+)
y1(-)
x2(+)
x2(-)
y2(+)
y2(-)
700b
700c
OPTICAL SIGNAL 700a

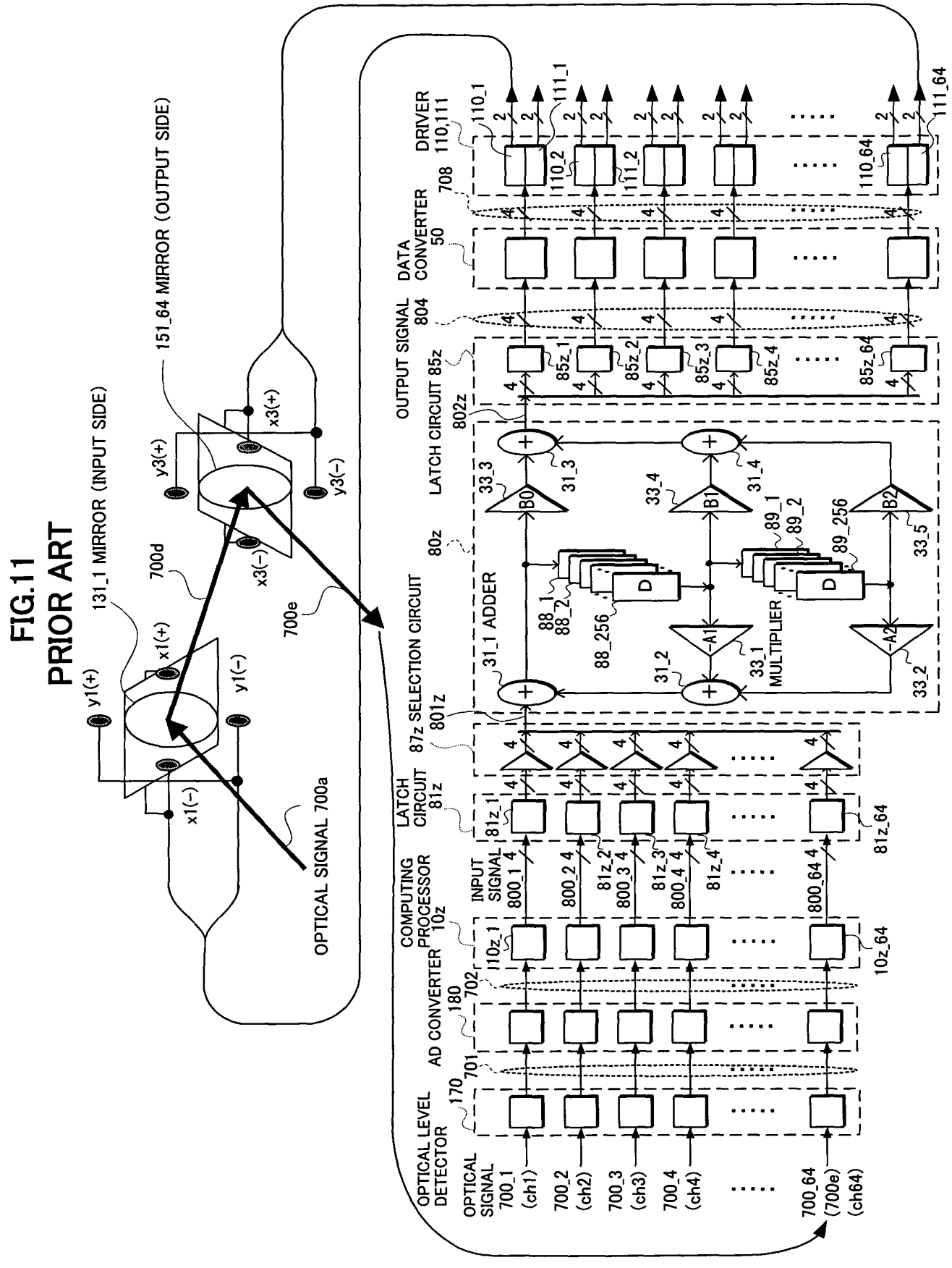



FIG.11
PRIOR ART